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. You can buy a license for Microsoft Windows, Macintosh or Linux. Accounts - Find/Change your Autodesk Account and manage your subscription and purchase options. . Terms of Use - Consult the License Agreement.This application is based upon and claims the benefit of priority from the prior Japanese Patent Application No. 11-097728, filed Mar. 23, 1999, the entire contents of which are incorporated herein by reference. The present invention relates to a semiconductor device having a non-volatile memory element and a method of manufacturing the same. The present invention relates to a non-volatile memory having a two-layer type floating gate, a metal-insulator-metal (hereinafter referred to as MIM) type non-volatile memory having a two-layer floating gate, and a method of manufacturing the same. Recently, a semiconductor device having a memory cell composed of a MISFET has been widely used. Among the MISFET, a MISFET formed on an SOI substrate, i.e. a silicon on insulator (SOI) substrate has been paid attention in recent years. The SOI substrate has advantages in that it has a low operating voltage, can operate at a high speed, and is resistant to soft errors due to radiation of particles. Therefore, the MISFET formed on the SOI substrate can be used in a high-reliability semiconductor device in which electric charges can be secured in each memory cell. In addition, a MISFET formed on the SOI substrate has a two-layer floating gate in which a control gate is buried in a floating gate. The two-layer floating gate can make the MISFET smaller and higher in the integration. Furthermore, it can decrease the influence of the spread of random noise. Therefore, the MISFET formed on the SOI substrate is widely used. In addition, there is provided a semiconductor device having a memory cell composed of a MISFET. Furthermore, the memory cell is composed of a selection MISFET and a memory MISFET. The selection MISFET is formed on a bulk substrate. A drain region and a source region of the selection MISFET are formed by diffusing an impurity into the bulk substrate. The source region and the drain region are formed by employing a self-alignment technique. On the other hand, the memory MISFET is formed on an SOI substrate. A drain region, a source

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